samples so as to improve testing performance, the semiconductor testing apparatus comprising:

an IDDQ measuring circuit configured to measure current data of good samples and the returned samples, by supplying test vector data to the good and returned samples;

a determination circuit configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data,

wherein the IDDQ measuring circuit tests the target semiconductor devices by applying the test vector data for the effective address pairs.

2. (Twice Amended) The apparatus of claim 1 wherein the determination circuit comprises:

a changing rate calculation circuit configured to select a plurality of address pairs from the test vector data, to supply the address pairs to the good samples and the returned samples, to measure current-values of the good samples and returned samples, and to calculate changing rates of each of the good samples and returned samples;

a range criteria determination circuit configured to determine the range of pass/fail decision criteria by using the changing rates of each of the good samples;

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a comparing circuit configured to compare the changing rates of each of the returned samples to the range of pass/fail decision criteria, and to determine whether the changing rates of each of the returned samples fall outside of the range of pass/fail decision criteria; and

an effective address pair determination circuit configured to determine the changing rate falling out of the range of pass/fail decision criteria, and to select an address pair which makes the returned samples to provide the changing rate falling outside of the range of the pass/fail decision criteria as the effective address pair.

3. (Twice Amended) The apparatus of claim 1, wherein the IDDQ measuring circuit comprises:

a tester configured to: acquire the effective address pair, supply the test data corresponding to the effective address pair to the target semiconductor device, measure current-value output of the target semiconductor device, and calculate changing rates of the target semiconductor device; and

a decision circuit configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

5. (Thrice Amended) A semiconductor testing method for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the method comprising:

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reading test vector data;

measuring current data of good samples and the returned samples by supplying the test vector data to the good and returned samples;

determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data; and

applying the test vector data for the effective address pairs to the target semiconductor devices for testing.

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6. (Twice Amended) The method of claim 5, further comprising:

selecting a plurality of address pairs from the test vector data;

supplying the address pairs to the good samples and the returned samples;

measuring current-values of the good samples and the returned samples;

calculating changing rates of each of the good samples and the returned samples;

determining a range of pass/fail decision criteria by using the changing rates of each of the good samples;

comparing the changing rates of each of the returned samples to the range of pass/fail decision criteria;

determining whether the changing rates of each of the returned samples fall outside of the range of pass/fail decision criteria;

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determining the changing rate falling outside of the range of pass/fail decision criteria; and

selecting an address pair which makes the returned samples to provide the changing rate falling outside of the range of pass/fail decision criteria as the effective address pair.

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7. (Twice Amended) The method of claim 5, further comprising:

acquiring the effective address pair;

supplying the test vector data corresponding to the effective address pair to the target semiconductor devices;

measuring current-value output of the target semiconductor devices;

calculating change rates of the target semiconductor devices; and

determining a changing rate falling outside of the range of pass/fail decision criteria.

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9. (Thrice Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, an IDDQ measuring circuit configured to test semiconductor devices by applying test vector data, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the program comprising:

instructions configured to read the test vector data;

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instructions configured to supply the test vector data to good samples and returned samples;

instructions configured to measure current data of the good and returned samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data; and

instructions configured to apply the test vector data for the effective address pairs for testing.

10. (Twice Amended) The program of claim 9, further comprising:

instructions configured to select a plurality of address pairs from the test vector data;

instructions configured to supply the address pairs to the good samples and the returned samples;

instructions configured to measure current-values of the good samples and the returned samples;

instructions configured to calculate changing rates of each of the good samples and the returned samples;

instructions configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

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instructions configured to compare the changing rates of each of the returned samples to the range of pass/fail decision criteria;

instructions configured to determine whether the changing rates of each samples fall outside of the range of pass/fail decision criteria;

instructions configured to determine the changing rate falling outside of the range of pass fail decision criteria; and

instructions configured to select an address pair that makes the returned samples to provide the changing rate falling outside of the range of pass/fail decision criteria as the effective address pair.

11. (Twice Amended) The program of claim 9, further comprising:

instructions configured to acquire the effective address pair;

instructions configured to supply the test vector data corresponding to the effective address pair to the target semiconductor devices;

instructions configured to measure current-value output of the target semiconductor devices;

instructions configured to calculate changing rates of the target semiconductor devices; and

instructions configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

13. (Thrice Amended) A semiconductor testing method of specifying a faulty part in a semiconductor device, configured to feed back data of returned samples which

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have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the method comprising:

reading a test program and test vector data;

supplying the test vector data to good and returned samples;

measuring current data of the good and returned samples, employing an IDDQ measuring circuit;

determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured current data;

applying the test vector data for the effective address pairs to a target semiconductor device; and

specifying a faulty part within the target semiconductor device by measuring an emission from the target semiconductor device.

14. (Twice Amended) The method of claim 13, further comprising:

selecting a plurality of address pairs from the test vector data;

supplying the address pairs to the good samples and the returned samples;

measuring current-values of the good samples and returned samples;

calculating changing rates of each of the good samples and returned samples;

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determining a range of pass/fail decision criteria by using the changing rates of each of the good samples;

comparing the changing rates of each of the returned samples to the range of pass/fail decision criteria;

determining whether the changing rates of each of the returned samples fall outside of the range of pass/fail decision criteria;

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determining the changing rate falling outside of the range of pass/fail decision criteria; and

selecting an address pair which makes the returned samples to provide the changing rate falling outside of the range of pass/fail decision criteria as the effective address pair.

15. (Twice Amended) The method of claim 14, wherein the faulty part specifying step further comprises:

acquiring the effective address pair;

supplying the test vector data corresponding to the effective address pair to the target semiconductor device;

measuring current-value output of the target semiconductor device;

calculating changing rates of the target semiconductor device;

measuring an emission from the target semiconductor device; and

determining a changing rate falling outside of the range of pass/fail decision criteria.

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16. (Thrice Amended) A semiconductor testing apparatus for specifying a faulty part in a semiconductor device, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the apparatus comprising:

a read circuit configured to read test vector data and a test program;

an IDDQ measuring circuit configured to measure current data of good samples and the returned samples, by supplying the test vector data to the good and returned samples;

a determination circuit configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process; and

a faulty part specifying circuit configured to apply the test vector data for the effective address pairs to the target semiconductor device and to specify a faulty part by measuring an emission from the target semiconductor device.

17. (Twice Amended) The method of claim 13, wherein determining a range of pass/fail decision criteria is achieved by:

a changing rate calculation circuit configured to select a plurality of address pairs from the test vector data, to supply the address pairs to the good samples and the returned samples, to measure current-values of the good samples and returned samples, and to calculate changing rates of each of the good samples and returned samples;

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a range criteria determination circuit configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

a comparing circuit configured to compare the changing rates of each of the returned samples to the range of pass/fail decision criteria, and to determine whether the changing rates of each of the returned samples fall outside of the range of pass/fail decision criteria; and

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an effective address pair determination circuit configured to determine the changing rate falling outside of the range of pass/fail decision criteria, and to select an address pair that makes the returned samples to provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

18. (Twice Amended) The method of claim 17, wherein the faulty part specifying circuit further comprises:

a tester configured to acquire the effective address pair, to supply the test vector data corresponding to the effective address pair to the target semiconductor device, to measure current-value output of the target semiconductor device, and to calculate changing rates of the target semiconductor device;

an emission measuring circuit configured to measure an emission from the target semiconductor device; and

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a decision circuit configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

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19. (Thrice Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the program comprising:

instructions configured to read a test program and test vector data;

instructions configured to measure current data of good samples and the returned samples, employing an IDDQ measuring circuit, by supplying the test vector data to good and returned samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured data;

instructions to apply the test vector data for the effective address pairs to the target semiconductor device; and

instructions to specify a faulty part within the target semiconductor device by measuring an emission from the target semiconductor device.

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